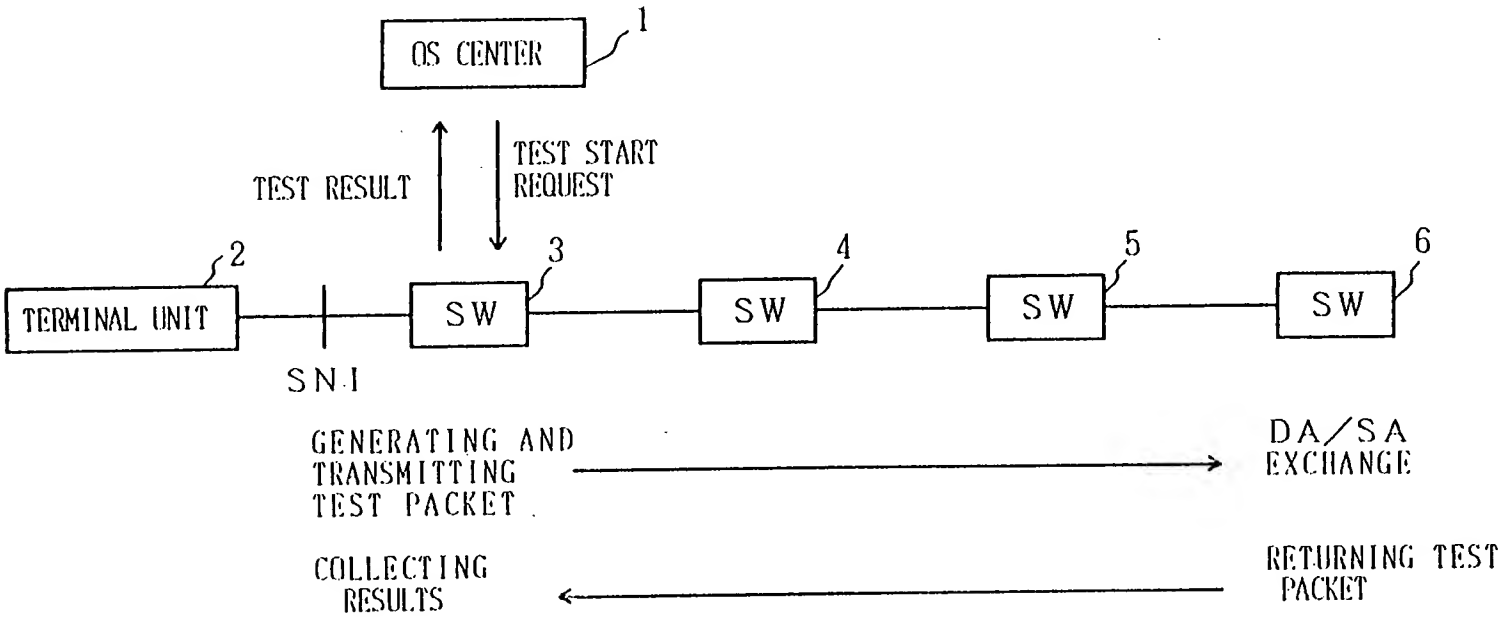



SH
O.K.

FIG. 898

(Prior Art)

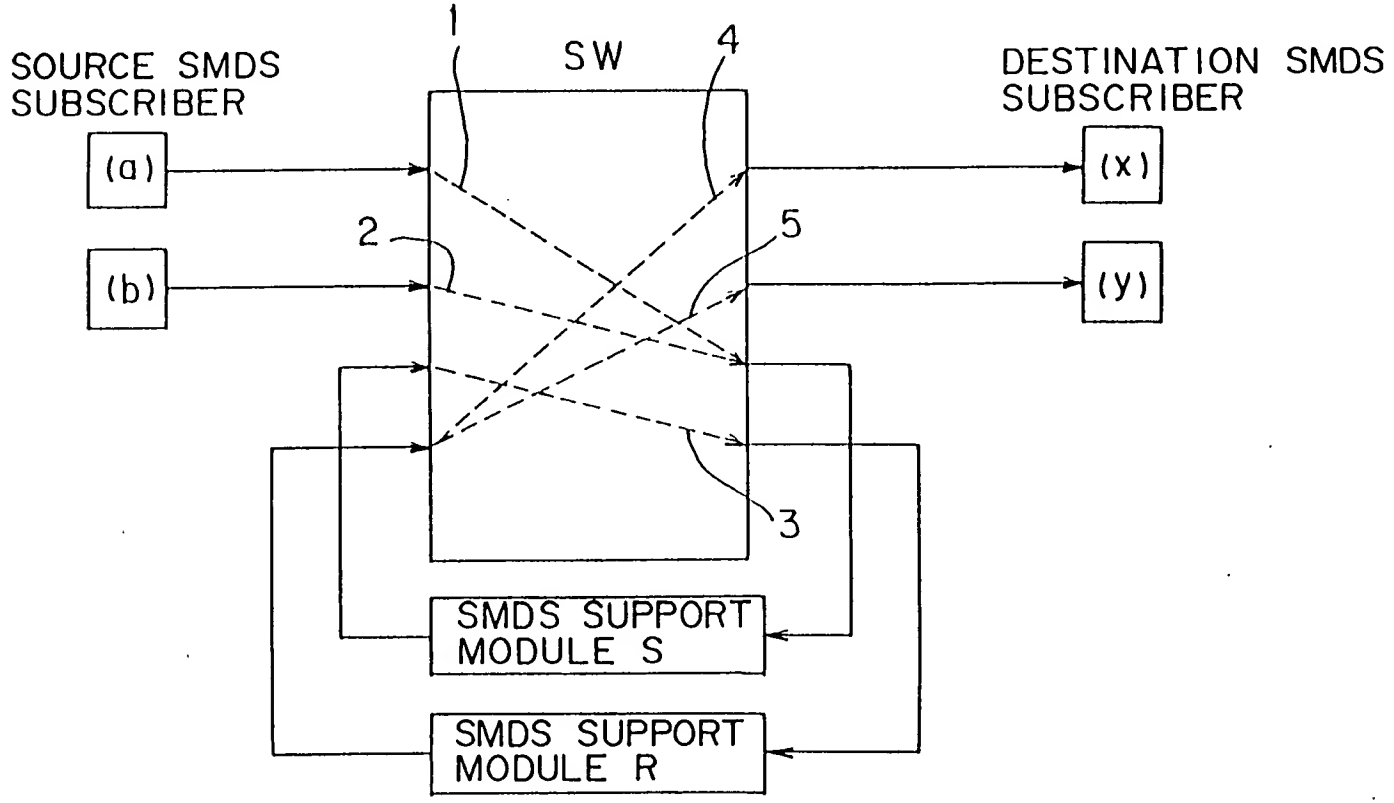
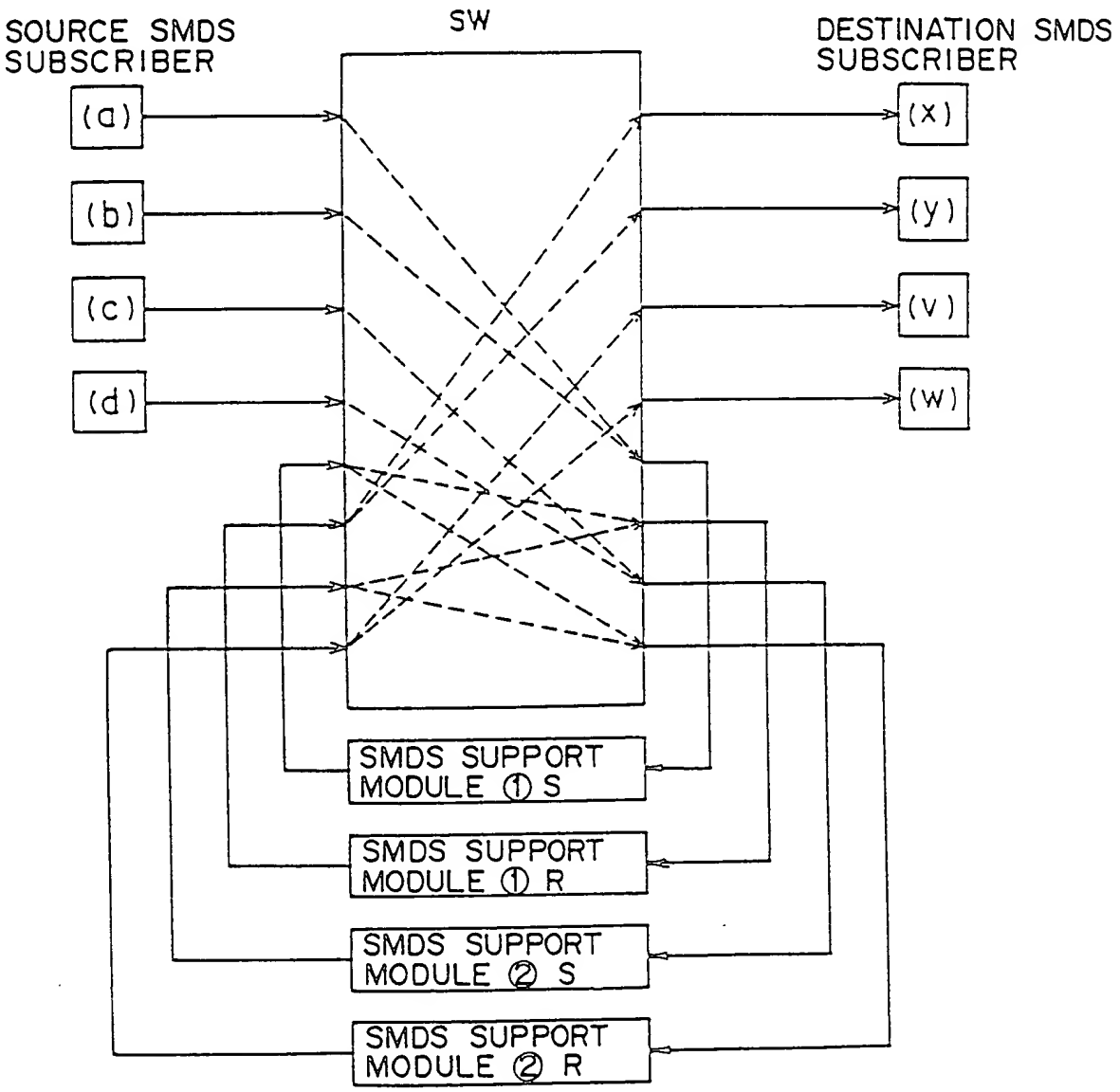


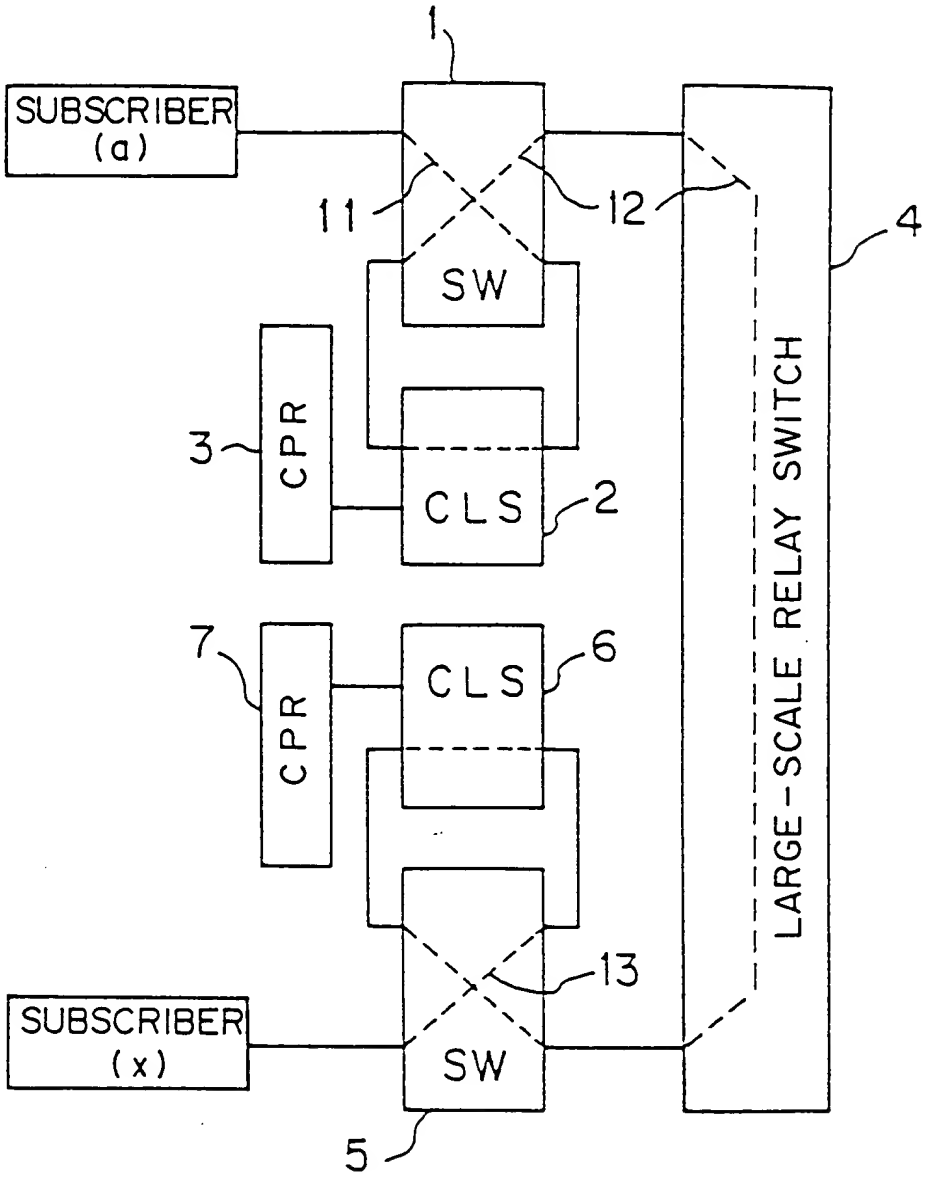

FIG. 899
(Prior Art)




SH
O.K.

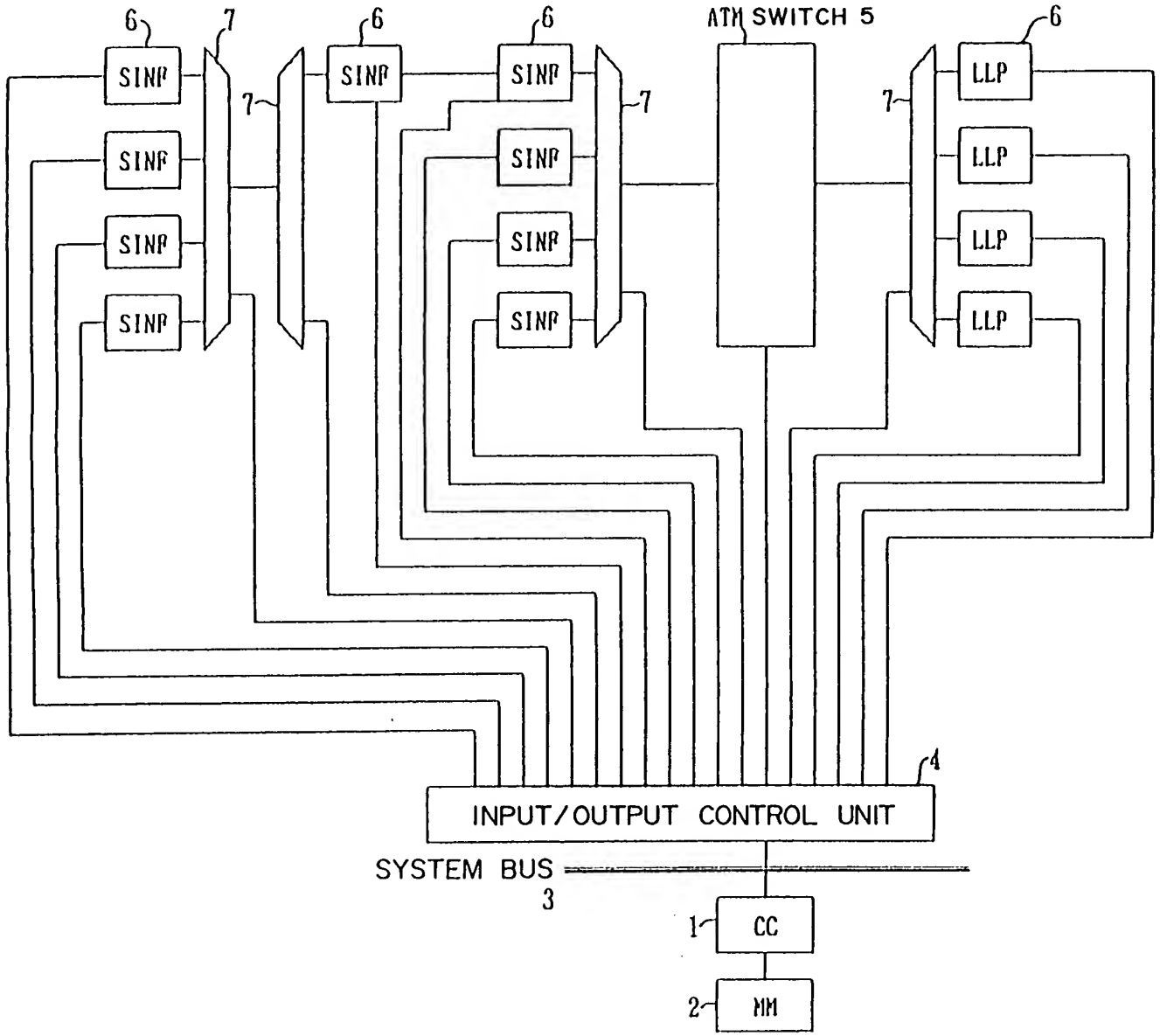
FIG. 900

(Prior Art)




SH
O.K

FIG. 901
(Prior Art)



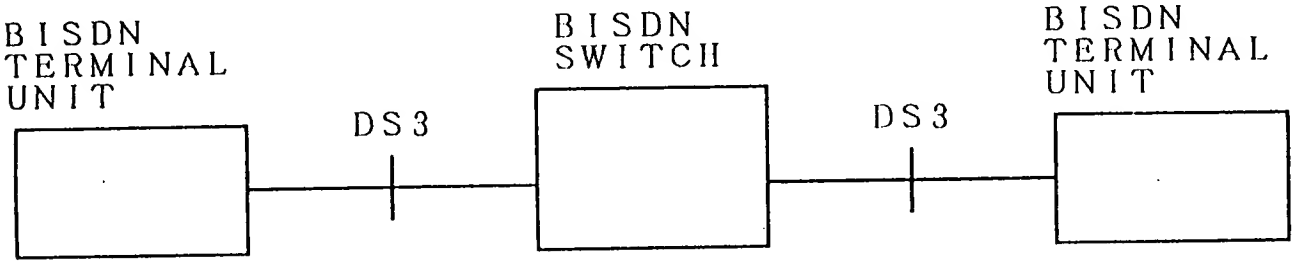

SH
O.K.

FIG. 902
(Prior Art)

SH
O.K.




FIG. 903
(Prior Art)




SH
O.K.

FIG. 904

(Prior Art)

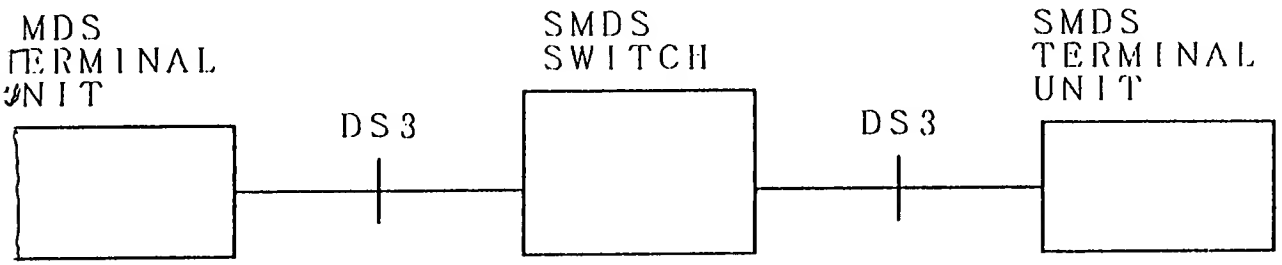
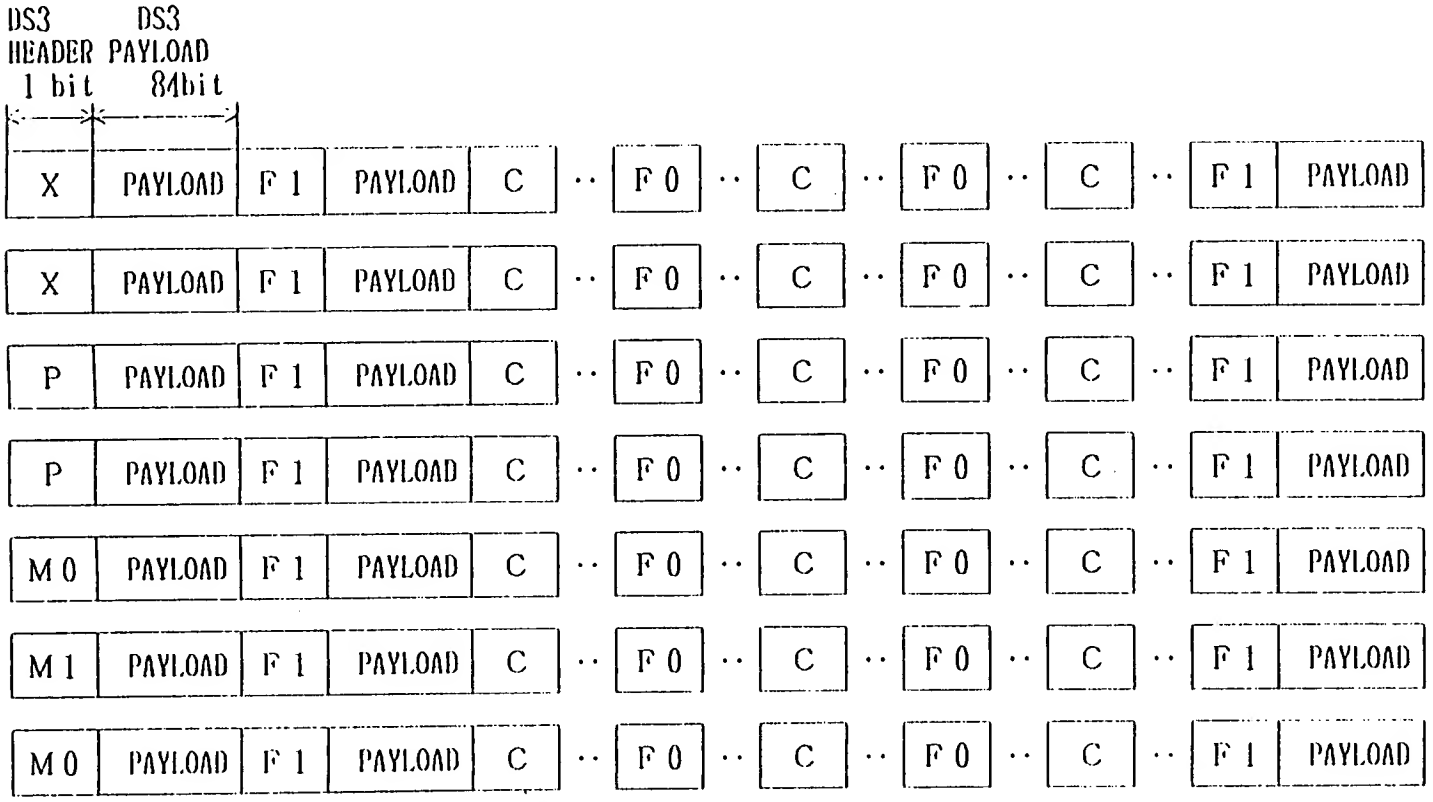



FIG. 905
(Prior Art)

SH
O.K.

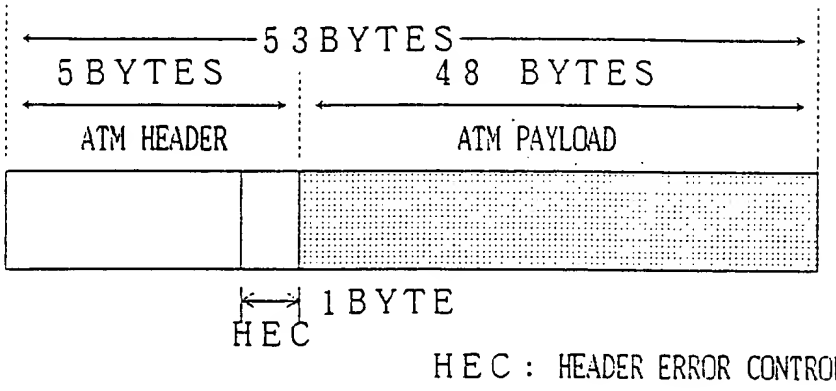



DS3 MULTIFRAME = 4760 BITS (85 BITS × 8 × 7)

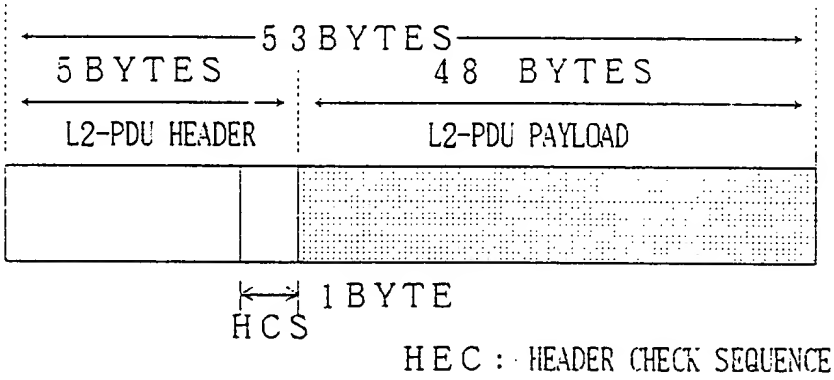
F0, F1 : SUBFRAME ALIGNMENT BIT
M0, M1 : MULTIFRAME ALIGNMENT BIT
P : PARITY INFORMATION BIT
X : ERROR STATE DESIGNATION BIT
C (RESERVED)

5H
O.K.

FIG. 906
(Prior Art)




(a) CONFIGURATION OF ATM CELL

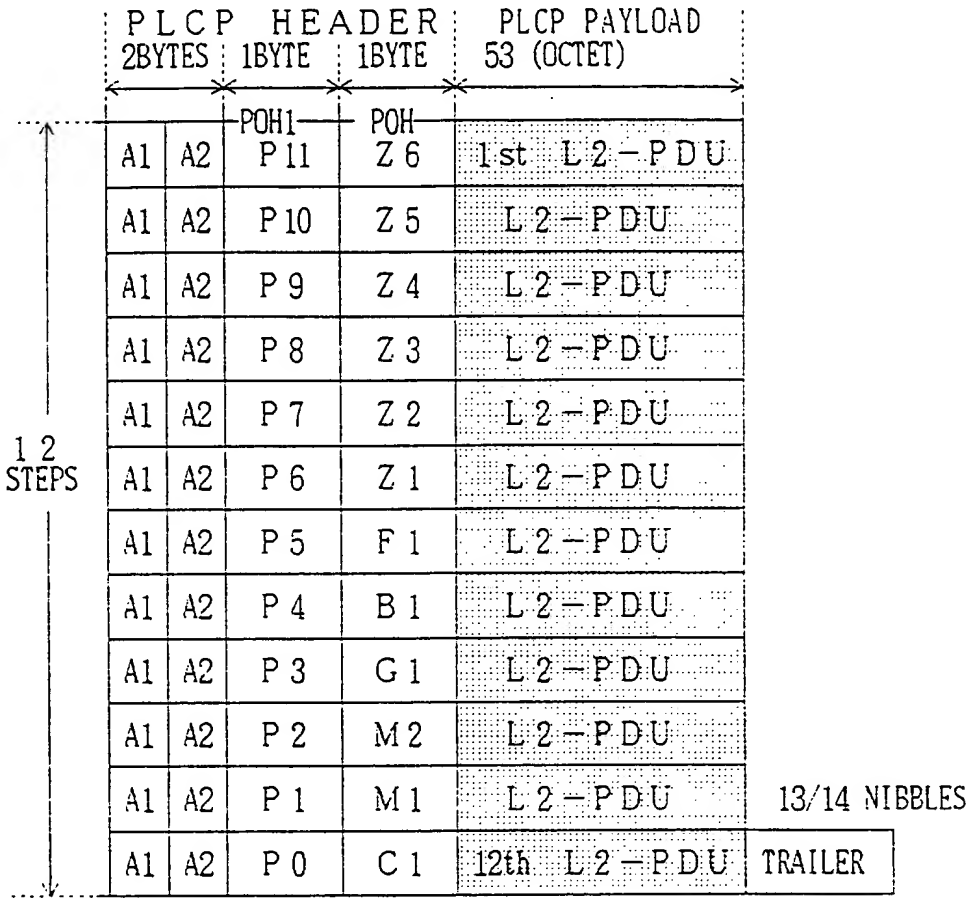



SH
O.K.

(b) CONFIGURATION OF SMDS CELL

FIG. 907

(Prior Art)



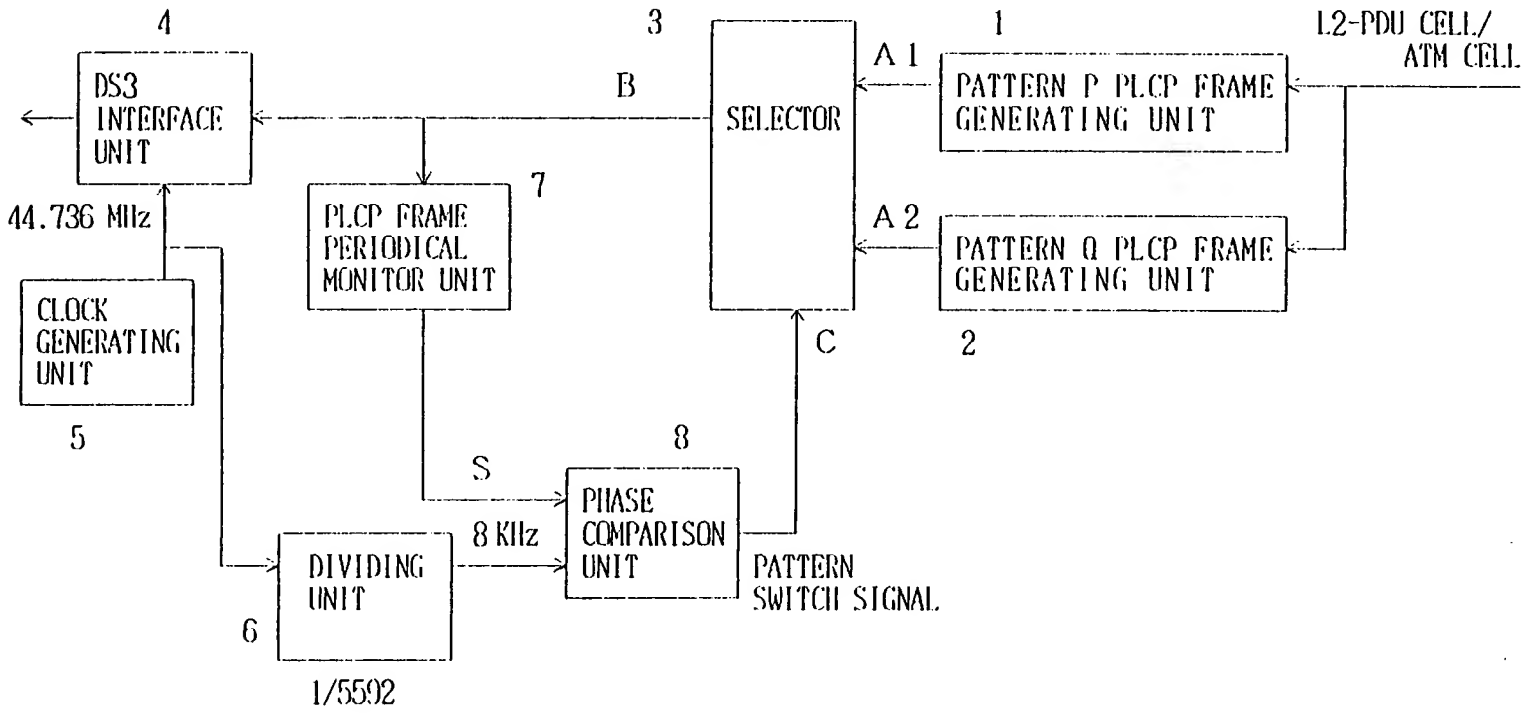

A1, A2 : FRAME ALIGNMENT
POHI (P11~P0) : PATH OVERHEAD IDENTIFIER OCTET
POH : PATH OVERHEAD OCTET
Z6~Z1 : GROSS OCTET
F1 : PLCP PATH USER CHANNEL
B1 : BIT INTERVAL PARITY 8
G1 : PLCP PATH STATUS
M2~M1 : SIP LEVEL 1 CONTROL INFORMATION
C1 : CYCLE STUFF COUNTER

FIG. 908
(Prior Art)

| ITEM | | BIT PATTERN | REMARKS |
|---|---|---|---|
| C1 | CYCLE STUFF COUNTER | | TL IS REPRESENTED BY 4 TYPES OF C1 AS SHOWN BELOW BECAUSE TRAILER LENGTH TL PERIODICALLY CHANGES IN DS3 PLCP FRAME. |
| | | 11111111 | ⟹ FIRST TYPE (TL=13) |
| | | 00000000 | ⟹ SECOND TYPE (TL=14) |
| | | 01100110 | ⟹ THIRD TYPE (TL=13 : NO STUFF) |
| | | 10011001 | ⟹ THIRD TYPE (TL=14 : STUFF) |
| TRAILER | | 1100 | LENGTH DEPENDS ON C1 BYTE VALUE. |

FIG. 909
(Prior Art)

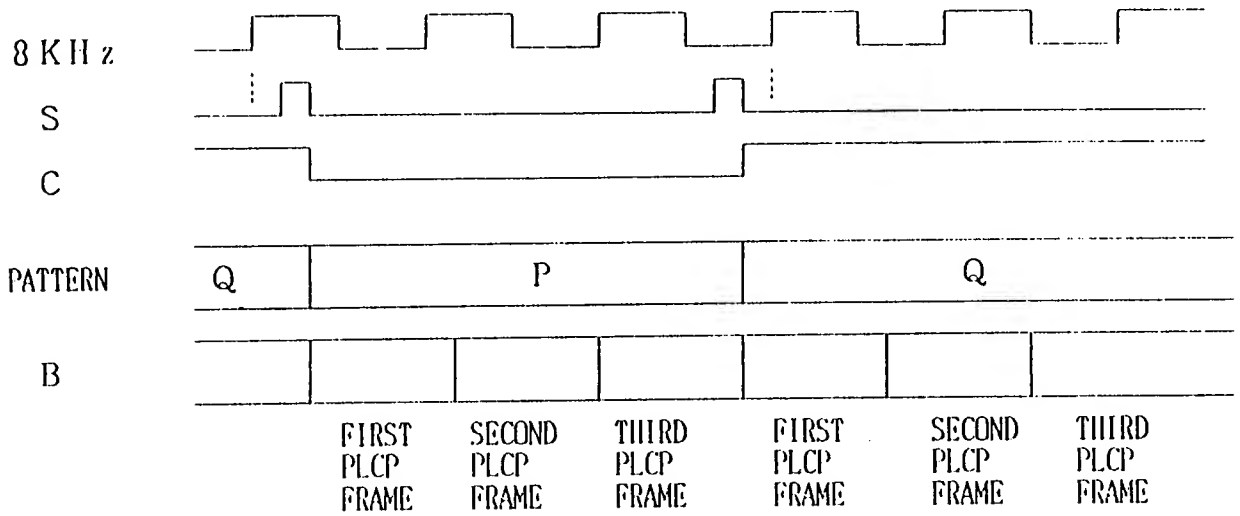
SH
O.K.




5H
O.K.

FIG. 910

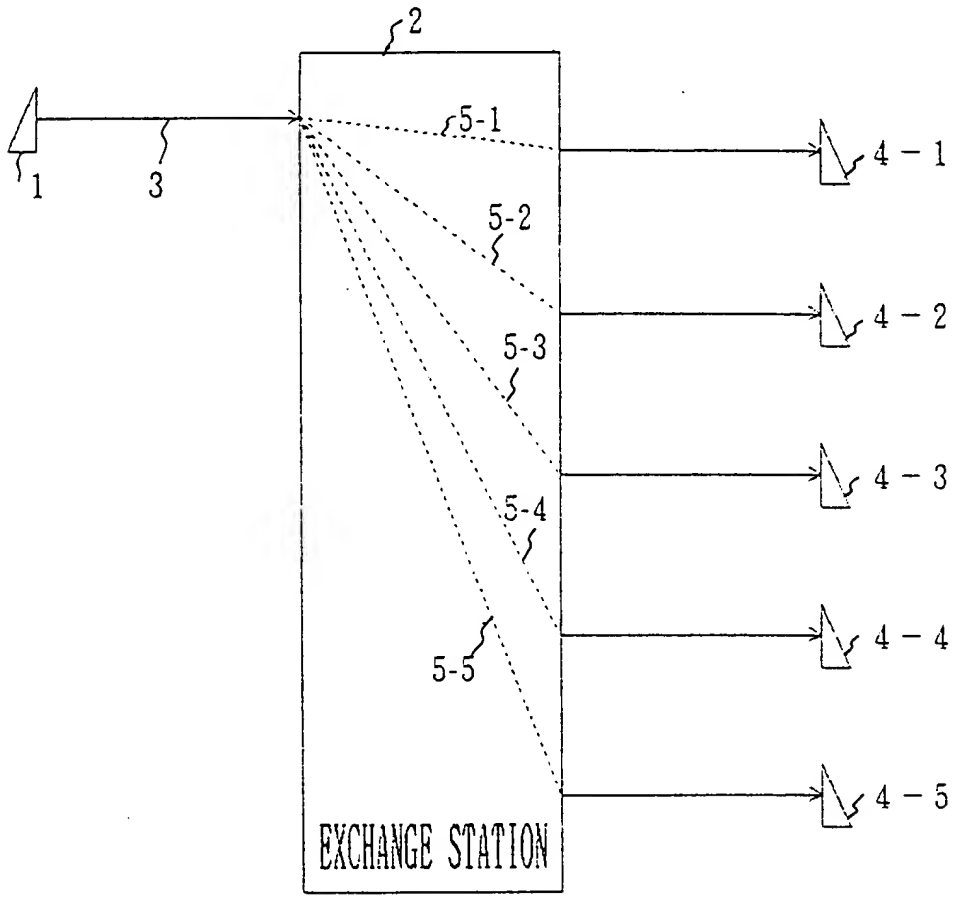
(Prior Art)




5H
O.K.

FIG. 911

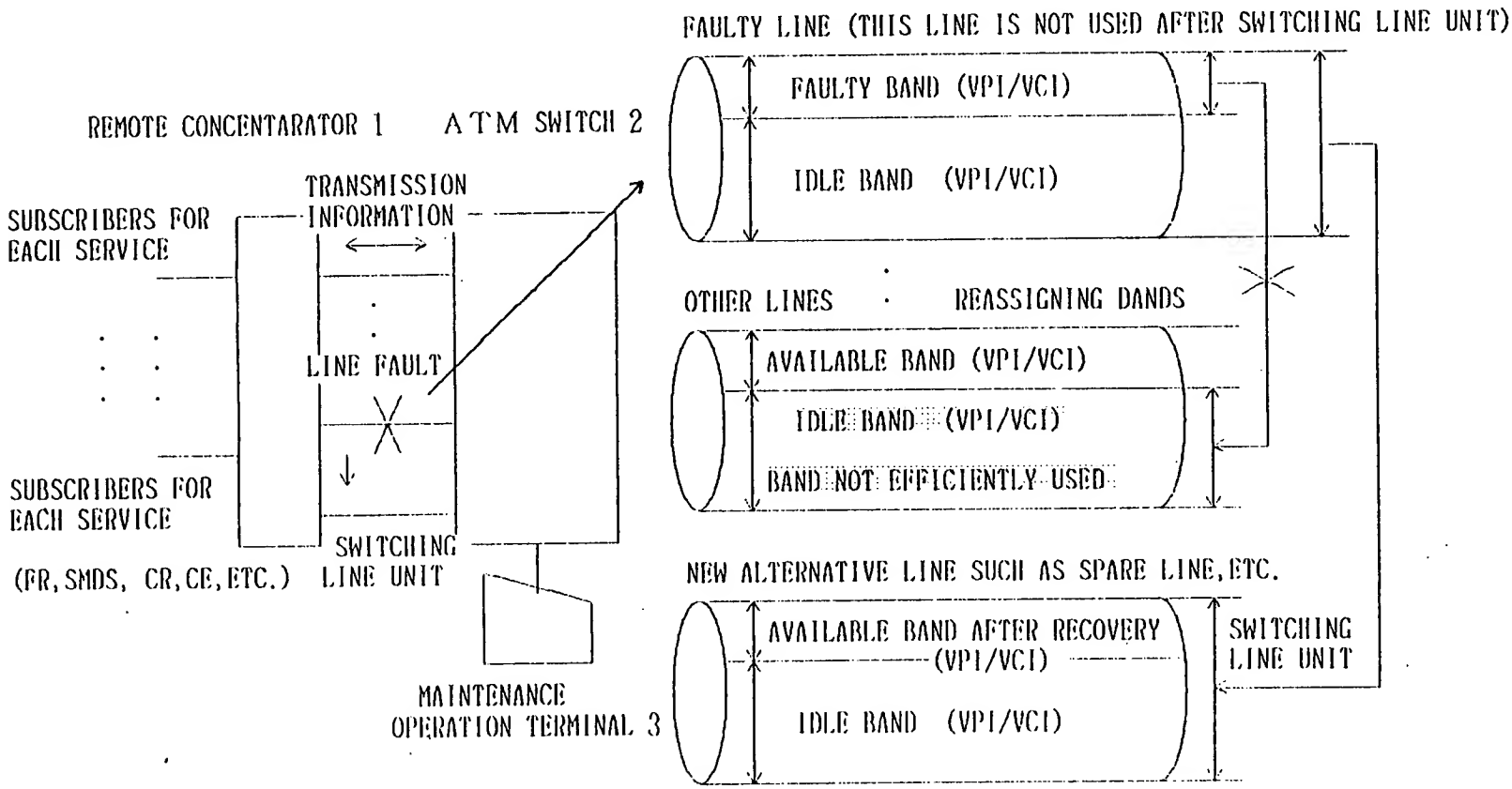
(Prior Art)




SH
O.IC.

FIG. 912

(Prior Art)




SH
O.K.

FIG. 913

(Prior Art)